Implementing An Efficient Full Adder using 3T XOR Gate for Low Power Applications

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Abstract - Due to the advancement in the technologies the increasing prominence of portable systems and the need to limit the power consumption in very high density vlsi chips have led to rapid and innovative developments in low power design during these recent years. The driving forces behind these developments are portable device applications requiring low power dissipation and high throughput, such as note book computers, portable communication devices and PDA (personal digital assistants). In most of these cases the requirements for low power consumption must be met along with equally demanding goals of high chip density and less area.

Basic building blocks of most of the arithmetic and logic circuits are formed by XOR logic gate. This paper proposes a new 3T-XOR gate with significant area and power savings. In most of the digital systems adder lies in the critical path that increases the overall computational delay of the system. And compares a couple of full adders one of them is proposed by using a multiplexer and another is a standard one in the terms of power consumption, area and delays and developing an efficient ripple carry adder using microwind tool.

I. INTRODUCTION

“CMOS” refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes. In our paper we have presented a brief review of Ripple Carry Adder using CMOS, along with comparing of the efficient full adder when compared with the standard full adder circuit basing the parameters of power, area and delays using microwind tool. Before designing a XOR gate using only three CMOS transistors.

II. ABOUT THE PAPER

In this paper we are going to implement a low power high performance and very efficient 3 transistor XOR gate and developing a full adder using this efficient XOR gate and the full adder is designed by using a 2x1 multiplexer for its high performance and very low delay when compared with the standard full adder in all the basic aspects of VLSI design. From this proposed efficient full adder considering the output results we then developing a best ripple carry adder using MICROWIND tool which is used for the CMOS designing and simulation.

MICROWIND is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to Design beyond their imagination. MICROWIND integrates Traditionally separated front-end and back-end chip design into an Integrated flow, accelerating the design cycle and reduced design Complexity. It tightly integrates mixed-signal implementation with digital Implementation, circuit simulation, transistor-level extraction and Verification – providing an innovative education initiative to help Individuals to develop the skills needed for design positions in Virtually every domain of IC industry.

The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the Microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. Designers can create logic circuits for Interfacing with these controllers and verify software programs using DSCH.

A. T-XOR Gate

The proposed new design of XOR logic gate using three transistors is shown in fig the design. The design is based on modified CMOS inverter and PMOS pass transistor logic. When the input Y is at logic one, the inverter on the left functions as a normal CMOS inverter. Therefore the output is the complement of input X. When the input Y is at logic zero, the CMOS inverter output is at high impedance. However, the PMOS pass transistor M3 is turned ON and the output gets the same logic value as input X. The operation of the whole circuit could be given as a 2 input XOR gate as given in Table.
Figure 1: 3T XOR gate

Exact output logic levels are obtained for all the input combinations without any voltage degradation. However, when X=0 and Y=0, voltage degradation due to threshold drop occurs across the PMOS pass transistor M3 while passing the output logic zero and consequently the output is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3 [9]. The equation (2) relates the threshold voltage of a MOS transistor to its channel length and width.

Figure 2: 3T XOR digital schematic

The proposed XOR gate was efficient low power powered and having a very less are with high performance and less delay. The layout when the Verilog code compiled in the microwind second module for layout generation and the results are indicated as shown in the graphical notation.

III. FULL ADDER MODULE

Full adder is one of the basic building blocks of many of the digital VLSI circuits. Several refinements have been made regarding its structure since its invention. The main aim of those modifications is to reduce the number of transistors to be used to perform the required logic, reduce the power consumption and increase the speed of operation.

Considering the standardized full adder the delay, power consumption and channel area are very high when compared with the proposed transistor which the proposed results are analyzed in the microwind tool a combination of DSCH and MICROWIND.in DSCH the digital schema of the CMOS circuit and in the second module the we can design the layout and also we can compile and execute the Verilog code. The standard circuit of the full adder is as shown in the following figure.

Figure 4: Digital schema of conventional full adder

Coming to the proposed full adder the number of device count is reduced as shown in the following pictorial representation containing two xor gates along with a 2x1 multiplexer. for the higher performance in different aspectsThe goal of this paper is to design a high performance and low power full adder module. The full adder operation can be given as follows: Given the three 1-bit inputs A, B, and C, it is desired to calculate the two 1-bit outputs Sum and Carry, The sum and carry expressions for one bit full adder is given by

\[ \text{Sum} = A \oplus B \oplus C, \quad \text{Carry} = AB + BC + CA. \]

The layout and the wave forms indicating the delay is as follows.
IV. PROPOSED FULL ADDER MODULE

In the proposed paper we are concentrating mainly on full adder implementation as it finds use in many of the low power applications. A basic full adder can be implemented with XOR gate, AND gates and OR gate. The logic for sum can be realized using XOR gate whereas the logic for carry can be realized using AND and OR gates. It shows that the entire full adder logic is based on its sum and carry outputs. Reducing the component counts in sum and carry logic may reduce the size of the full adder. For that purpose a 3 transistor XOR gate has been proposed which uses only two pMOS transistors and one nMOS transistor to perform the required logic similar to two input XOR gate.

In the proposed logic, the full adder is designed with a minimum of two XOR gates and a multiplexer which is a modified version of the existing. It uses both the pMOS and nMOS transistors in its hardware circuitry. The 3 transistor XOR gate plays a dominant role in minimizing the component count from 5 to 3. In addition to XOR gate the proposed full adder also used one which can be obtained by modifying the basic equations of sum and carry of a full adder which also plays an important role in minimizing the device count.

The proposed full adder when designed in the digital schematic editor of microwind tool is as shown in the fig the inputs are represented with switches and the output values are determined by using LED’s when they are on it indicates the output as 1 and if the LED is off when it indicates the 0 value.

V. RIPPLE CARRY ADDER MODULE

An N-bit adder can be constructed by cascading N full adders, these are also called as carry ripple adder or ripple carry adder. A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded with the carry output from each full adder connected to the carry input of the next full adder in the chain. Shows the interconnection of four full adder circuits to provide a 4-bit ripple carry adder. From Figure that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Half adders can be used to add a two bit numbers Bits and in the figure represent the least significant bits of the numbers to be added. This configuration is called a ripple carry adder since the carry bit “ripples” from one stage to the other. The delay through the circuit depends upon the number of logic stages that must be traversed and is a function of applied input signals at the input terminals of the circuit of the schema. In the ripple carry adder, the
output is known after the carry generated by the previous stage is produced. Thus, the sum of the most significant it is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay.

The ripple carry adder which is developed by using the full adders using multiplexers is as follows and the each full adder is converted in to single symbol of full adder and then these 4 symbols are cascaded for the forming of a ripple carry adder. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry are the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output.

![Figure 10: Digital schema of ripple carry adder](image)

![Figure 11: Layout for ripple carry adder](image)

The layout of the developed ripple carry adder is as follows in which the Verilog code is compiled for layout extraction and there is another method to design the layout manually similar to designing the digital schematic of the circuit in the DSCH window. It is better to compile the Verilog code than manually designing a layout by using each and every layer for the exact layout to the digital schema. The waveform which represents the time and voltage characteristic is as shown in the fig 12. The output characteristics of a circuit is obtained when the simulation is processed in the microwind window we can get the output characteristics at each and every output terminals of the circuit.

![Figure 12: Characteristics of ripple carry adder](image)

A. Result Analysis

The various results of all the above discussed circuits are described in the detailed manner in the following tabular forms.

<table>
<thead>
<tr>
<th></th>
<th>3-tor xor</th>
<th>Full adder using mux</th>
<th>Standard full adder</th>
<th>Ripple carry adder</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption</td>
<td>0.562 uw</td>
<td>6.155 uw</td>
<td>7.861 uw</td>
<td>11.792 uw</td>
</tr>
<tr>
<td>area</td>
<td>90 um</td>
<td>168 um</td>
<td>180 um</td>
<td>676 um</td>
</tr>
<tr>
<td>delay</td>
<td>15ps</td>
<td>5ps &amp; 61ps</td>
<td>1023ps &amp; 25ps</td>
<td></td>
</tr>
</tbody>
</table>

VI. CONCLUSION

In this paper, we have presented a systematic approach to construct full adder using only 3 transistor XOR cell. The proposed approach resulted in low power consumption can be reduced nearly to 25% and high speed compared to the existing full adder architectures. According to MICROWIND simulation in 16 nm CMOS process technology at room temperature, and under given conditions, the proposed full adder shows an improvement of power consumption over conventional CMOS adder, also area is also less when compared with the conventional full adder. In addition, the delay and power-delay product results depict impressive improvement over conventional CMOS adder.

REFERENCES

[1] CMOS vlsi design by neil neste, david harris and Aryan benerjee.